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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/856,853	05/25/2001	Akihiko Ito	109158	4755
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25944 7590 02/13/2003

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EXAMINER

ABDULSELAM, ABBAS I

ART UNIT

PAPER NUMBER

2674

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/856,853

Applicant(s)

ITO, AKIHIKO

Examiner

Abbas I Abdulsalam

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 24-46 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 24-46 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-23 has been canceled by the applicant and claims 24-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scheffer et al. (USPN 5852429).

Regarding claims 24 and 30, Scheffer teaches LCD matrix display system (10) including pixels (26) and a frame period (T). See Fig 1. Scheffer teaches gray scale method of addressing display (12) including a pulse width modulation where several frame periods T of the display information are used to control the duration of the time that the pixel is "on" compared with the time the pixel is "off" (col. 25, 18-23 and 39-44). Scheffer, in connection to pulse width modulation, teaches the time "on" and "off" information state of a pixel with respect to each time interval  $\Delta t_k$  being subdivided into G smaller time intervals  $\Delta t_{kg}$  (col. 25, lines 45-67.) see Fig. 20. Furthermore, Scheffer teaches that electrode pattern as shown in Fig 1 comprises multiple rows and columns from which a pixel is formed at the intersection (col. 5, lines 38-43). However, Scheffer does not specifically disclose turning "on" or "off" the pixels in the second time period in accordance with a threshold of voltage. Scheffer on the other hand teaches mathematical equations to calculate the use voltage across the pixel. For example, Scheffer teaches averaging the pixel voltage over a frame period, calculating ratio of the

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magnitude of the peak voltage occurring a given state of the pixel, and illustrating the “on” and “off” states of pixel with respect to “on” and “off” RMS voltage across the pixel. See col. 6, lines 55-67 (equations 5& 6), and col. 14, lines 21-46 (equations 37 and 38).

Therefore, it would have been obvious to one having skill in the art at the time the invention was made to utilize Scheffer's equations (5, 6, 37, 38) used to establish the amount of voltage applied in a pixel during a frame period. One would have been motivated in view of Scheffer that manipulating the equations would provide the desired threshold voltage. The use of scheffer's equations helps function gray scale display system as taught by Scheffer.

Regarding claim 25-26 and 31 Scheffer teaches a voltage waveform across a pixel for several frame periods as well as optical response of a pixel to the voltage waveforms. See Fig 7 and Fig 8.

Regarding claims 27-29 and 32-35, Scheffer teaches a display matrix (12) along with column and row signal generators and a swift function generator (96), which provides sequential swift function vector to row driver, IC 98. See col. 19, lines 1-14 and Fig 12. In addition, Scheffer teaches row and column addressing signals applied to LCD matrix including “on” and “off” states of pixel with respect to a period T. See Fig 1.

2. Claims 36-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. (USPN 5892495) in view of Scheffer et al. (USPN 5852429).

Regarding claims 36, 38-39 and 41, Sakai teaches a matrix crystal type liquid crystal display panel (1) including multiple data lines (DL), multiple scanning lines (SL), a data line driving circuit (2), a scanning line driving circuit (3) and pixel (5) composed of a switching

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element (SW). Sakai teaches that the data line (DL) and the electrode of the pixel capacitor  $C_p$ , that is, a pixel electrode  $E_p$  are connected with the switching element SW. Sakai teaches that the scanning line driving circuit (3) sequentially selects the scanning lines (SL) and controls the closing and opening of the respective switching elements (SW) in the pixels (col. 9, lines 20-56 and Fig 2(a)). In addition, Sakai teaches the switching element for outputting the picture signal supplied from data lines to the pixel electrodes in accordance with the selection signal supplied to the scanning lines (col. 7, lines 65-67, col. 8, lines 1-4). Sakai teaches the scanning circuit with respect to a period of time required for sampling the picture as well as the data line driving circuit (2) sequentially selecting the picture signals inputted during a period of a predetermined duration and supplies signals to the data lines (col. 6, lines 52-62 and col. 9, lines 54-56).

However, Sakai does not teach the scanning line with respect to a single frame time and sub-fields. Sakai also does not teach a data line-driving circuit with respect to signals "each designating turning on or off each pixel in accordance with a gray-scale level of respective pixels. Scheffer as discussed above teaches the time "on" and "off" information state of a pixel with respect to each time interval  $\Delta t_k$  being subdivided into  $G$  smaller time intervals  $\Delta t_{kg}$  (co. 25, lines 45-67 and Fig 7, Fig 20). Sakai also teaches the use of a frame period ( $T$ ) with respect to row and column signals of the LCD display (12) (col. 5, lines 12-24 and 50-53).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify Sakai's display system to include Scheffer's frame and pulse width modulation techniques that is used to control the state of pixels (26). One would have been motivated in view of the suggestion in Scheffer that frame and pulse width modulation technique

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equivalently provides the desired frame time along with the state of pixels (on and off). The use of frame and pulse width modulations helps function LCD display panel as taught by Scheffer.

Regarding claims 37 and 40, Sakai teaches an address signal with respect frequencies and time required for reading data corresponding to each pixel. See col. 6, lines 25-34.

Regarding claims 42-44, Sakai teaches an imaging system with respect to multiple scanning lines orthogonally crossing the data line so as to sequentially select the pixel electrodes to be supplied with the picture signal. See col. 7, lines 15-19.

Regarding claims 45-46, Sakai teaches a display system where in the pixel electrodes, the elements, and the data line driving circuit are provided on either amorphous silicon thin film or monocrystalline silicon film formed on insulating substrate. See col. 8, lines 5-9.

### **Conclusion**

3. The prior art made of record and not relied upon is considered to applicant's disclosure.

The following arts are cited for further reference.

U.S. Pat. No. 6,462,724 to Ozawa et al.

U.S. Pat. No. 6,433,763 to Lim et al.

U.S. Pat. No. 6,429,836 to Hansen

U.S. Pat. No. 6,414,664 to Conover et al.

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4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulsalam** whose telephone number is **(703) 305-8591**. The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709**.

**Any response to this action should be mailed to:**

Commissioner of patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314**

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulsalam

Examiner

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**RICHARD HJERPE**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2600**